RESUME

Name: DIPIKA SIMARIYA
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E-mail: deepikasimariya02@gmail.com

CAREER OBJECTIVE:

By acquiring knowledge, expertise and a familiarity with the organization's culture, I want to contribute towards realizing organization's vision and become its integral part.

EDUCATIONAL QUALIFICATION:

Qualification	School / Institute	Board / University	Year	% /c.g.p.a
M.Tech- Microelectronics &VLSI Branch (0801EI18MT04)	Shri G.S Institute of Technology and Science	R.G.P.V	2018-2020	8.71
B.E-EC Branch (0802EC121033)	Shri Vaishnav Institute of Technology & Science	R.G.P.V	2016	7.47
12th passout	Sarafa Vidya Niketan	M.P Board	2012	86%
10th passout	Shri Nath High School	M.P Board	2010	75.4%

COMPUTER / TECHNICAL SKILLS:

Languages:

Basics of C & C++ (Turbo C++)

VHDL & **Verilog** (Altera 9.1 version & Xilinx)

Basics of **Embedded C** & **PCB Designing** (Keil uvision & Proteus)

Knowledge of **Mentor Graphics** and **Cadence Software**.

MAJOR TRAININGS:

1) Summer training on FPGA using Verilog from Shri Vaishnav Institute of Technology and Science.

2) 15 days vocational training on Global System for Mobile Communication from VEDANG PVT. LTD.

THESIS WORK

1) Pulse Start-up Based Low Power Wideband Class C VCO (**M.Tech**).

2) Automatic College Bell using 8051 microcontroller using Embedded C Programming (**B.E**).

CONFERENCE / JOURNAL PUBLICATIONS

1) Dipika Simariya, R.C. Gurjar, D.K. Mishra, "Pulse Start-up Technique Based Class C VCO using 180nm CMOS Technology" Department of Electronics and Instrumentation Engg., SGSITS Indore, M.P., India, ***5th International Conference on Microelectronics and Computing Systems (MCCS-2020) 11th-12th July 2020 at ARTTC BSNL, Ranchi, Jharkhand, India,*** **pp. 175.**

2) Dipika Simariya, R.C. Gurjar, D.K. Mishra, "Low Power Wideband Class C VCO using 180nm CMOS Technology" Department of Electronics and Instrumentation Engg., SGSITS Indore, M.P., India, ***ICTACT Journal on Microelectronics, Volume 6 (IJME0644-under process)***

OTHER MAJOR ACEDMIC ACHIEVEMENTS (GATE/GRE/NET):

1) UGC NET (DEC 2019) Qualified

2) GATE 2018 Qualified

PERSONAL DETAILS:

Date of Birth	**:** 2 JUNE 1995
Father's Name	**:** Naresh Simariya
Language Known	**:** English, Hindi
Address	**:** D-1729 Sudmanagar, Indore (M.P.)

DECLARATION:

I hereby declare that all the above mentioned information given by me is true and correct to the best of my knowledge and belief.